1. **a)** Config 1 provides the least costly configuration with the 128kB cache. The reason for this because in a 1-way cache, you will end inevitably end up with block collisions and polls to L2/main memory, which means block will be constantly swapped in and out of L1 for the majority of the runtime. However, given that associativity and size are literally factors in the cost of the L1 cache, the overall system cost increases when you add the cost of checking tags, as well as supporting the various extra blocks of cache. Therefore, while config 1 certainly does not provide the best simulation runtime, it provides the most cost-efficient use of L2.

**b)** The overall data miss rate does not change, and increasing L2’s size will not change that. This is because L2 is accessed only when a cache miss occurs on L1, which does not depend on L2’s configuration in any way, especially since the total number of L2 accesses is a subset of the L1 accesses, equaling the L1 misses.

**c)** Increasing L2 from 128kB to 256kB does not change the simulation time for any of the configurations, which implies that the 128kB L2 was large enough to accommodate the data requests sent to it from L1 misses.